

Introduction: Sintered lunar soil has been proposed as a basic construction material [1] for such diverse applications as roadways, launch pads, dust control, thermal and radiation protection, and basic construction elements such as bricks, columns, panels, etc. as part of an In-Situ Resource Utilization (ISRU) effort. Various methods of sintering have been explored including simple radiant heating [2], microwaves [3], and focused solar energy [4].

Sintering involves the controlled melting at the grain boundaries to produce optimum mechanical properties. However, it is possible to over-sinter with excessive heating and/or duration [5]. For example, optimally sintered lunar soil simulant JSC-1A is mechanically strong and robust, and of moderate density, while over-sintered JSC-1A (melted) is brittle and overly dense. As little as 25°C can make the difference between minimal sintering and total melting [2].

An in-situ electronic monitoring approach is used to develop an “electronic signature” of optimally sintered material to essentially know when to stop heating. Previously, this was largely a cut-and-try approach, dependent on starting material (JSC-1A, MLS-1, etc.), particle size distribution, and size and shape of the green body.

Impedance Spectroscopy [6] was originally considered as it is often used to analyze grains and interfaces (grain boundaries) of ceramics [7] and composites [8]. However, the sintering process evolves too quickly, especially in microwave heating, and the multi-frequency analysis process is unnecessarily complex. Monitoring a single frequency (1 kHz) and noting its departure from a predicted Arrhenius plot of ionic conduction, provides a simple method for end-point detection.

Theoretical Background: We consider a parallel plate electrode capacitive sensing arrangement with the lunar soil simulant placed between the plates. The following equivalent circuit [6, 9] can be drawn:

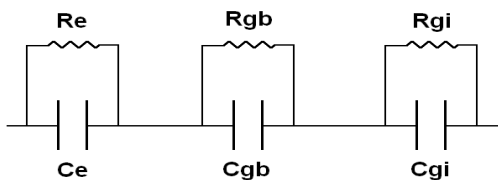


Figure 1. Equivalent circuit to measure impedance
e=electrode, gb=grain boundary, gi=grain interior.

where R_e , R_{gb} and R_{gi} , and C_e , C_{gb} and C_{gi} are the RC circuit elements corresponding to the electrode, grain boundaries, and grain interfaces respectively. Typically, [9, 10] the grain interior has the lowest capacitance, followed by the grain boundary, and then the electrodes. These values may differ by an order or orders of magnitude. While the resistance elements are typically of the same order of magnitude, their value is highly temperature dependent and given by the Arrhenius equation [11]:

$$\sigma = A/T e^{-E_a / K_b T} \quad (1)$$

where σ is the conductivity, A is the pre-exponential constant, T is the temperature, E_a is the activation energy, and K_b is Boltzmann's constant. The Arrhenius equation is best visualized by taking the natural logarithm of both sides of equation (1):

$$\ln(\sigma) = \ln(A/T) - (E_a/K_b) (1/T) \quad (2)$$

An Arrhenius plot is then graphed using $\ln(\sigma)$ on the y-axis and $1/T$ on the x-axis. Under ideal conditions, the graph is a straight line whose slope is $-E_a/K_b$ and y-intercept is $\ln(A/T)$. However, there are conditions where the Arrhenius plot may deviate from a straight line [12].

Consider the initial heating of the JSC-1A where increasing temperature provides increasing thermal energy to mobile ions, hopping through defects, to create a conduction current. As a general rule, for every 10°C increase in temperature, the conduction will double. As we approach the onset of sintering, the contact area between grains increases, lowering the value of R_{gb} in figure 1. From this point onward as the temperature continues to rise, the conduction current will increase both through increasing thermal activation, and from increasing contact area between grains. The slope of the Arrhenius graph will increase, giving rise to a “convex” Arrhenius plot. Once the JSC-1A has completely melted, only thermal activation will, from that point onward in temperature increase, contribute to the increasing conductivity.

Experimental Setup: To test this idea, a simple setup was constructed using a 20 ml high-alumina combustion boat (CoorsTek P/N 65566) and a parallel plate capacitive electrode sensor. This sensor is made from two strips of type 304 stainless steel each 75mm long, 12mm wide and 0.1 mm thick and is separated by two ceramic insulators each 19mm long and 6.4mm in diameter, fastened to the ends of the parallel strips. Type 304 stainless steel wires 0.5mm in diameter are

used to make external connections. The combustion boat and capacitive sensor are shown in figure 2.



Figure 2. Combustion boat and capacitive sensor. Once the capacitive sensor is placed in the boat, JSC-1A is added until it is level with the top of the boat, with light tamping to level the surface as shown in figure 3. A typical charge is 28.4 grams.



Figure 3. Combustion boat with sensor and JSC-1A. An in-house constructed tube furnace was used, consisting of a Mullite tube 457mm (18") long with and ID of 31.75mm (1.25") with a 304.8mm (12") hot zone wound with Kanthal A1. Multiple mica end zone baffles provide a $\pm 5^\circ\text{C}$ uniformity over the central 203mm (8") at a maximum operating temperature of 1175°C . The loaded boat and baffles are shown being placed into the tube furnace in figure 4.

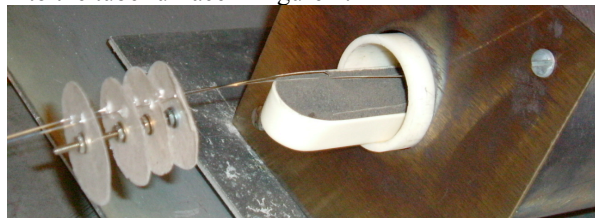


Figure 4. Boat and baffles being placed into furnace. Conductivity was measured with a Sinometer VC6243 LC meter operating at 1kHz and 500mVpp.

A Hitachi 4800 Scanning Electron Microscope (SEM), provided by Brookhaven National Lab's Center for Functional Nanomaterials was used to image JSC-1A, and figure 5 shows it in a highly sintered state.

Analysis: Figure 6 shows the Arrhenius plot of the sintering of JSC-1A which has a relatively linear graph up to point A (about 1009°C) where melting begins. Melting is near complete from point B (about 1143°C) to point C (about 1175°C , the furnace maximum). Optimum sintering will likely occur over interval A-B.

Conclusions: This initial investigation sought to demonstrate the feasibility of developing an electronic signature which tracks the sintering process as it occurs, and develop an end point detection for optimum

sintering. Future work will try to correlate specific sintering morphologies with an electronic signature.

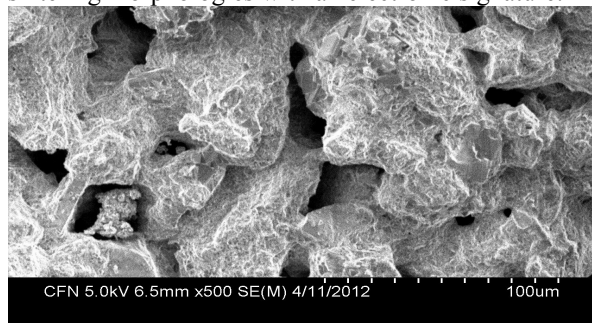


Figure 5. JSC-1A sintered for 1 hour at 1075°C .

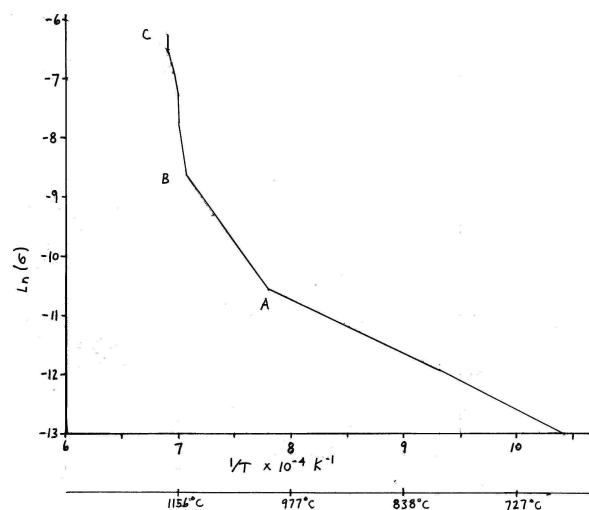


Figure 6. Arrhenius plot of the sintering of JSC-1A.

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References: [1] Shirley F. et al. (1989) *A Preliminary Design Concept for a Lunar Sintered Regolith Production Facility*, Battelle, Columbus, Ohio. [2] Allen C. A. et al. (1992) *Proc. Space '92*, 2, 1209-1218. [3] Taylor L. A. and Meek T. T. (2005) *J. Aerosp. Eng.* 18, 188-197. [4] Smith B. (2010) *SRR/PTMSS*. [5] German R. M. (1996) *Sintering Theory and Practice*, John Wiley and Sons, NY. [6] Barsoukov E. and Macdonald J. R. (2005) *Impedance Spectroscopy*, John Wiley and Sons, NY. [7] Muccillo R. (2009) *J. Mater. Res.*, 24,5, 1780-1784. [8] Talla J. A. et al. (2011) *J. Mater. Res.* 26,22, 2854-2859. [9] Bauerle J. E. (1969) *J. Phys. Chem. Solids* 30, 2657-2670. [10] Bauerle J. E. (1976) *Electrochim. Acta* 21, 303-310. [11] Bruce P. G. (1997) *Solid State Electrochemistry* Cambridge University Press, NY. [12] Truhlar D. G. and Kohen A. (2001) *PNAS* 98,3, 848-851.